Whether the functionality is implemented as hardware or software depends upon the particular application and design constraints imposed on the overall system. Skilled artisans recognize the interchangeability of hardware and software under these circumstances, and how best to implement the described functionality for each particular application.

As examples, the various illustrative logical blocks, modules, circuits, and algorithm steps described in connection with the embodiments disclosed herein may be implemented or performed with a Digital Signal Processor (DSP), an Application Specific Integrated Circuit (ASIC), a Field Programmable Gate Array (FPGA) or other programmable logic device, discrete gate or transistor logic, discrete hardware components such as, e.g., registers and First In First Out (FIFO) type, a processor executing a set of firmware instructions, any conventional programmable software module and a processor, or any combination thereof designed to perform the functions described herein. The processor may advantageously be a microprocessor, but in the alternative, the processor may be any conventional processor, controller, microcontroller, or state machine. The software modules could reside in Random Access Memory (RAM), FLASH memory, Read Only Memory (ROM), Electrically Programmable ROM (EPROM) memory, Electrically Erasable Programmable ROM (EEPROM), registers, hard disk, a removable disk, a Compact Disk-ROM (CD-ROM), or any other form of storage medium known in the art. The processor may reside in an ASIC (not shown). The ASIC may reside in a telephone (not shown). In the alternative, the processor may reside in a telephone. The processor may be implemented as a combination of a DSP and a microprocessor, or as two microprocessors in conjunction with a DSP core, etc.

The previous description of the preferred embodiments is provided to enable any person skilled in the art to make or use the present invention. The various modifications to these embodiments will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other embodiments without the use of the inventive faculty. Thus, the present invention is not intended to be limited to the embodiments shown herein but is to be accorded the widest scope consistent with the principles and novel features disclosed herein.

We claim:

**1**. A mobile station comprising:

a processor configured to:

receive a broadcast-to-pilot ratio from a base station;

determine a normalized data rate as a function of the received broadcast-to-pilot ratio and a power of a pilot signal received from the base station; and

a transmitter configured to transmit the normalized data rate to the base station.

**2**. The mobile station of claim **1**, wherein the processor is further configured to receive a data rate indicator from the base station, the date rate indicator based on the transmitted normalized date rate.

**3**. The mobile station of claim **2**, further comprising:

a receiver configured to receive traffic from the base station at a date rate indicated by the data rate indicator.

**4**. A mobile station comprising:

means for receiving a broadcast-to-pilot ratio from a base station;

means for determining a normalized data rate as a function of the received broadcast-to-pilot ratio and a power of a pilot signal received from the base station; and

means for transmitting the normalized data rate to the base station.

**5**. The mobile station of claim **4** further comprising:

means for receiving a data rate indicator from the base station, the date rate indicator based on the transmitted normalized date rate.

**6**. The mobile station of claim **5** further comprising:

means for receiving traffic from the base station at a date rate indicated by the data rate indicator.

**7**. A method of operating a mobile station comprising:

receiving a broadcast-to-pilot ratio from a base station;

determining, by said mobile station, a normalized data rate as a function of the received broadcast-to-pilot ratio and a power of a pilot signal received from the base station; and

transmitting, by said mobile station, the normalized data rate to the base station.

**8**. The method of claim **7** further comprising:

receiving a data rate indicator from the base station, the date rate indicator based on the transmitted normalized date rate.

**9**. The method of claim **8** further comprising:

receiving traffic from the base station at a date rate indicated by the data rate indicator.

**10**. A non-transitory processor-readable medium memory having instructions thereon executable by a processor, the instructions comprising:

code for receiving a broadcast-to-pilot ratio from a base station;

code for determining a normalized data rate as a function of the received broadcast-to-pilot ratio and a power of a pilot signal received from the base stations; and

code for transmitting the normalized data rate to the base station.

**11**. A non-transitory processor-readable medium memory of claim **10** further comprising: code for receiving a data rate indicator from the base station, the date rate indicator based on the transmitted normalized date rate.

**12**. A non-transitory processor-readable medium memory of claim **10** further having comprising: code for receiving traffic from the base station at a date rate indicated by the data rate indicator.

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